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## Description

### Background of the Invention

This invention relates to programmable logic integrated circuits. In particular, the invention relates to a new architecture which provides for greater utility and flexibility of programmable logic devices ("PLDs"), and allows for programmable logic devices of much greater complexity than previously were possible.

The following references are background to this invention: Hartmann et al. U.S. patent 4,617,479; Hartmann et al. U.S. patent 4,609,986; Veenstra U.S. patent 4,677,318; Hartmann et al. U.S. patent 4,713,792; Birkner et al. U.S. patent 4,124,899; Cavlan U.S. patent 4,703,206; Spencer U.S. patent 3,566,153; J. C. Leininger, "Universal Logic Module", IBM Technical Disclosure Bulletin, Vol. 13, No. 5, October 1970, pp. 1294-95; Ronald R. Munoz and Charles E. Stroud, "Automatic Partitioning of Programmable Logic Devices", VLSI Systems Design Magazine, October 1987, pp. 74-78, and 86; and E. Goetting et al., "A CMOS Electrically-Reprogrammable ASIC with Multi-Level Random Logic Capabilities", 1986 IEEE International Solid State Circuits Conference (Proceedings), pp. 244, 245, 359, and 360.

Several approaches have been used for the architecture of programmable logic integrated circuits. Among these are the "programmable AND, fixed OR" structure (referred to as a PAL) used in the above-mentioned Birkner et al. patent. This architecture has the advantages of higher speed and a simpler structure. However, because it has a fixed number of "product terms" (hereinafter "P-terms") per OR logic function (eight P-terms is typical of most current PAL products), and because these P-terms cannot be shared by neighboring OR gates, many P-terms are typically wasted. On the other hand, there are occasions when eight P-terms are not enough to handle the more complex logic functions. Experience has shown that in a broad range of applications, eight P-terms is on average much more than enough, and yet it is also often insufficient. For example, FIG. 2 in the above-mentioned Munoz et al. article is a graph of P-term requirements for a relatively large sample of logic functions (Munoz et al. FIG. 2 is substantially reproduced herein as FIG. 1). Similar studies done by the assignee of the present invention arrive at roughly similar conclusions: namely, a large percentage of logical functions (on the order of 50 to 70 percent) require less than four P-terms. However, a relatively significant "tail" exists where eight P-terms is not enough.

One way to achieve higher P-term utilization is to provide "variable P-term distribution". In essence, this is an attempt to guess a mixture of P-term requirements such that some OR gates have few P-

terms (e.g., four), and some have a relatively large number (e.g., 12 or 16). See, for example, above-mentioned U.S. patent 4,609,986. This partially solves the problem of P-term utilization, but it significantly increases the complexity of the software support task because each function must be examined and then, depending upon its demand for P-term resources, assigned to a specific macrocell which has the minimum resources needed to fulfill the required demand (this process is called "fitting"). However, even with variable P-term distribution, many P-terms are typically still wasted.

Another way in which this P-term allocation problem can be solved is suggested in the above-mentioned paper by Leininger. With this structure, the P-term array is viewed as an array of programmable NOR or NAND gates whose inputs are programmable. Functions which require more than a single P-term are broken into multi-level NAND (or NOR) functions. Each level of (e.g., NAND) logic takes one P-term. Using this type of array, even quite complex logic functions can be done in a few levels of NAND logic. Again, however, there are some drawbacks. First, it is very likely that most logic functions will take more than a single P-term. This means that most often, several passes through the array will be required, and this causes a slowing down of evaluation of the function. Second, each P-term must feed back into the array input section. Thus, as the number of P-terms grows, so does the number of input lines. Even for arrays of modest complexity, the number of input signal lines (sometimes called "word lines") becomes excessive. For example, the part described in the above-mentioned IEEE ISSCC paper has only eight macrocells but has nearly 100 word lines, while a PAL circuit of similar complexity has only half as many word lines. Each word line adds to the length (and therefore the parasitic capacitance) of all of the P-terms. Greater P-term length leads to slower signal propagation.

Finally, there are programmable logic arrays ("PLAs") of the type described in the above-mentioned Spencer patent. Most (if not all) functions can be accomplished in one pass through the "AND" array plus one pass through the "OR" array. However, even the simplest functions require these two array delays. Thus, compared to the PAL architecture, there is a speed penalty (at least for simple functions). This type of PLA circuit is also more complex to execute in silicon because of the need for interface buffering between the AND and the OR array, and because of the inherently more complex programming circuits needed to program the two arrays.

In prior art programmable logic devices, a major obstacle to increasing the logic density has been array sizes which increase as the "square" of the increase in the number of output functions. This is true because for complete generality, it is necessary that all output functions also feed back as inputs into the

array. However, in practice, it has been observed that this is massive overkill. That is, on average, only some subset of functions needs to be fed back. One solution to this problem is to break a single large array into several smaller arrays with functional communication between the smaller array blocks. In prior art devices such as the EP1200 (see U.S. patent 4,609,986) and the EP1800 (both commercially available from Altera Corporation of Santa Clara, California), this interconnect between blocks was done in a fixed manner by providing multiplexers which select and route outputs of one logic array block, or input signals, to one of the word line conductors of the other of said array blocks. That is, in a device with several array blocks, there is local feedback to an array block, and there are a certain fixed number of global feedback signals between array blocks. While this approach does serve to keep the array sub-blocks to reasonable size (both from a bit density and a speed point of view), it creates routing bottlenecks between blocks. For example, in the Altera EP1800, there are four array blocks each with 12 flip-flop macrocells. Only four macrocell outputs from each array block are routed as global inputs to the other blocks. This bottleneck causes significant restrictions in allowing logic functions to "fit" within a device even though there are enough other resources (such as flip-flops, I/O pins, etc.).

The paper "Programmable logic devices come of age" by S.KOPEC published in Electro /87 and Mini/micro Northeast Conference Record, April 7-9, 1987, New York, US, pages 19/0/1 - 19/0/6 teaches the use of feedback programmable interconnect segments between macrocells, with a fixed interconnect net, without however giving any detail as to its implementation.

In view of the foregoing, it is an object of this invention to provide an architecture for programmable logic devices which allows for the implementation of PLDs of much greater complexity.

It is another object of the invention to maximize the utilization of P-terms in PLDs.

It is a further object of the invention to make PLDs of high complexity that can operate at high speed.

It is a further object of the invention to provide for multiple logic array blocks ("LABs") which can operate independently or in concert, and to provide for a programmable interconnect array ("PIA") structure which allows for ease of communication between these array blocks.

It is a further object of the invention to provide a macrocell which is simpler and provides for increased functionality.

It is a further object of the invention to provide a regular, repeatable architecture which will be easy for a user to understand and easy for software tools to support.

It is a further object of the invention to provide for

a modular architecture which allows for ease in constructing a family of products simply by reducing or increasing the number of LABs and the associated PIA structure.

It is a further object of the invention to allow for package bonding options such that some of the I/O pins are not bonded out, thus allowing high density PLDs to be put into relatively low pin-count packages.

## Summary of the Invention

According to the invention there is provided a programmable logic device including first and second logic array blocks each including a plurality of word line conductors, a plurality of P-term line conductors each of which is programmably interconnectable to at least some of said word line conductors for producing on each P-term line conductor a signal which is a logical function of the signals on the word line conductors, and means for deriving output signals from at least one of said P-term line conductor signals of at least said first logic array block, a programmable interconnect array being provided for selectively applying said output signals to any of a plurality of the word line conductors of the second of said logic array blocks characterised in that said programmable interconnect array comprises a plurality of word lines each of which receives a respective one of said output signals, a plurality of bit lines perpendicular to said word lines each of which bit lines is connected to a respective one of said plurality of the word line conductors of said second of said logic array blocks and programmable elements at the intersection of said word lines and bit lines for selectively programmably connecting each of said bit lines to any one of said word lines.

The present invention solves all of the above-mentioned P-term allocation problems, and in addition provides a programmable interconnect array structure which allows the implementation of much larger programmable logic devices (PLDs) than have heretofore been possible. Reference will now be made to the following elements present in the preferred embodiments of the present invention:

1. The logic array block ("LAB") best seen in Fig 3.
2. The macrocell/flip-flop block best seen in Fig 5.
3. The programmable interconnect array ("PIA") best seen in Fig 3.
4. The input/output circuit best seen in Fig 5.
5. The clock functions best seen in Fig 5.

## A. The Logic Array Block (LAB)

As mentioned above, the present invention increases the utilization of P-terms. Most functions (eg counters, demultiplexers, 2 to 1 and 4 to 1 multiplexers, and shift registers, as well as any simple AND,

OR, NAND, or NOR function) can be done in one pass through the array. Many more complex functions which require three P-terms or less and which can directly utilize the EXCLUSIVE-OR (XOR) gate can also be done directly in a single pass through the array. This accounts for approximately 70% of the logic functions that are found in most logic designs. The remaining functions which require additional product terms can be done by using "expander" P-terms which (in combination with the three-P-term programmable AND, fixed OR, XOR) can produce very complex NAND-NAND, AND-OR, OR-AND, and NOR-NOR types of functions. The general advantage of this combined structure is that a majority of logic functions can be done in one pass through the array (thus achieving maximum speed), and even the most complex functions can be done in two passes.

#### B. The Macrocell/Flip-Flop Block

The output of the above-mentioned AND-OR-XOR structure feeds a flip-flop logic block. In prior art circuits such as the Altera EP300 (see U.S. patent 4,617,479) this is typically a conventional D flip-flop with a mechanism for allowing the flip-flop register to be optionally bypassed to allow the combinational output to be applied directly to the output section if desired. In the device described herein, this structure has been modified such that the multiplexer and attendant control formerly required to bypass the flip-flop are no longer necessary. In place of the old structure a new flip-flop structure has been incorporated which allows operation as a D flip-flop, a level-sensitive latch, or a completely flow-through device which allows combinatorial functions to be directly propagated. A preferred structure for this new flip-flop is described in US-A-4 864 161.

#### C. Programmable Interconnect Array (PIA)

The device of this invention solves the routing bottleneck problem by the creation of a programmable interconnect array (PIA) which allows any logic function output and any of the I/O input signals to be input to any of the logic array blocks (LABs). With this programmable interconnect array structure in place, the LABs can be kept to sizes which are functionally convenient, modular, and have a reasonable number of programmable elements. While all logic function outputs and the I/O inputs are taken into the PIA (a total of 180 word lines in the case of the device depicted in FIG. 3), only a subset (24 in the case of the present devices) are programmably routed as inputs into each of the logic array blocks. Unless an LAB requires more than 24 such inputs (which is highly unlikely), this architecture allows for completely general routing of signals.

#### D. Input/Output

In most prior art programmable logic devices, certain package pins are designated as inputs and others as outputs (see, for example, the MMI 16R8, commercially available from Monolithic Memories Incorporated (now merged with and part of Advanced Micro Devices ("AMD") of Sunnyvale, California). An improvement on this has been the use of tri-state buffers in conjunction with a feedback path from the I/O pin back into the array such that when the output buffer is in its tri-state condition, the pin may be used as an input (see the above-mentioned Birkner et al. patent). This mechanism provides for flexibility of usage of pin resources. However, when the I/O buffer is tri-stated and the associated pin is used as an input, the associated output macrocell logic is lost. This is a waste of precious resources. A solution to this problem is provision for "dual-feedback" such as that found on certain pins of the Altera EP1800. Dual feedback provides a feedback path both from the I/O pin and from its associated logic macrocell. Thus when the output buffer is tri-stated, the I/O pin can be used as an input and the macrocell resource can still be used as a "buried" register. In the present device, this mechanism is further improved in that I/O pin feedback does not go directly into the array, but rather is an input to the PIA. Thus I/O input lines can go to any or all of the LABs, while at the same time the logic macrocell function can be used (1) locally as feedback to its own LAB, and (2) globally via the PIA. Thus I/O pin functions are effectively decoupled from the logic arrays. This provides for much greater utility and flexibility than was heretofore possible.

#### E. Clock Functions

Generally, the register functions in PLDs are clocked either synchronously (for example, see the MMI 16R8) or asynchronously (see the MMI 20RA10). In most systems, there is a need for both types of capabilities. A solution to this problem is the structure that has been used in the Altera EP600, EP900, and EP1800. In these devices a multiplexer has been provided which allows the user to select either the synchronous (global) clock signal or an "asynchronous" (local P-term) clock. This selection can be made on a macrocell-by-macrocell basis. However, this multiplexer structure adds to the complexity of the device, and the additional circuitry needed to make the selection adds delay to the clock signal. An improved approach has been taken in the present device which allows for a simple clock gating of the "global" synchronous clock with a local P-term. If the synchronous clock is desired, then the asynchronous clock P-terms are programmed such that they are always low. This allows the global clock signal to pass to the flip-flop. If asynchronous clocking is desired, the global

clock signal is forced low (again by programming) and the local clock P-term is allowed through to clock the flip-flop. The clock selection (i.e., synchronous versus asynchronous) is done on a per LAB basis. This structure completely eliminates the clock multiplexer and the controls for same. This new structure is simpler and faster.

Further features of the invention, its nature and various advantages will be more apparent from the accompanying drawings and the following detailed description of the invention.

#### Brief Description of the Drawings

FIG. 1 is a chart showing typical product term distribution (frequency of occurrence of logic functions requiring a given number of product terms to implement the same) for a large sample of PLD designs.

FIG. 2 is a prior art programmable logic circuit macrocell.

FIG. 3 is a block diagram of an illustrative embodiment of the present invention.

FIG. 4 is a block diagram of one section of the embodiment of FIG. 3 showing one logic array block (LAB) and one programmable Interconnect array block (PIA).

FIG. 5 is a logical representation of a (macrocell) portion of an LAB in the embodiment of FIGS. 3 and 4.

FIGS. 6a (comprising parts 6a and 6aa) and 6b (comprising parts 6b and 6bb) are diagrams showing two "bond out options" for the device shown in block diagram form in FIG. 3.

FIG. 7 is a block diagram of an alternative embodiment having fewer LABs than the device shown in FIG. 3.

FIGS. 8a through 8h illustrate the way in which logic functions of varying complexity can be fit into the macrocell of the present invention.

FIG. 9 is a truth table useful in explaining the operation of a new flip-flop-type element used in the device of this invention.

#### Detailed Description of the Preferred Embodiments

FIG. 3 is an overall block diagram of an illustrative embodiment of a programmable logic device 10 constructed in accordance with the present invention. The major elements shown in this diagram are "fast inputs" 30, I/O pads 40, logic array blocks (LABs) 50, and programmable interconnect array (PIA) blocks 60.

Input signals into chip 10 come from either fast inputs 30 or I/O inputs 40. Fast inputs 30 are routed via lines 31 to all of LABs 50. These signals drive into the array portion of the LAB through buffers 57 which provide both the true and complement polarity of the signal presented to the fast input pad. These lines are

called fast inputs because they go directly to the LABs, in contrast to I/O inputs 40 which go indirectly to the LABs via PIA blocks 60. This can be seen by following representative signal line 41 from the pads labeled I/O0:7 (which represent eight such I/O pads) to buffer 42. After the signal has been suitably buffered by buffer 42, it drives into the PIA along line 43. By means of programmable elements 63 which are at the intersection of PIA word lines 43 and Interconnect term lines 61, a signal which originated at one of the I/O pads 40 can be routed to any LAB 50 via the interconnect term 61 through buffer 58 and then into a true/complement LAB word line buffer 57. Signals propagating to an LAB via this path take additional time to traverse the PIA. Hence these signals are "slower" than the "fast" input lines 31 which go directly to the LAB as explained above. The reasons for providing these two different paths will be explained in due course.

A typical LAB 50 will now be explained in more detail. In this architecture there can be as many LABs as is deemed desirable. For example, in various preferred embodiments implemented to date we have used either four or eight LABs.

Each LAB 50 comprises macrocells 51 and expanders 52. Inputs to the LAB are provided by fast inputs via buffers 57, PIA inputs via interconnect terms 61 through buffers 58 and 57, feedback terms from macrocell outputs via buffers 54 and 57, and expander feedback terms via buffers 55 and 56. Two types of macrocells are provided. The only difference is the inclusion of output buffers 53 (plus their associated output enable (OE) signal 110 which provides the output tri-state control) in macrocells 1 through 8. Output buffers 53 selectively apply the associated macrocell outputs to I/O signal pins 40. Macrocells 9 through 16 have no associated output buffer and are therefore sometimes referred to as "buried" macrocells. In either case, the macrocells all have buffers 54 which take the signal generated by the macrocell and feed it to its own LAB (as described above) and also drive PIA word lines 62.

In the preferred embodiment shown in FIG. 3, each LAB 50 has 16 macrocells, 32 expanders, eight fast inputs, and 24 array inputs from the interconnect terms of the PIA. Each LAB also has a number of tri-state output drivers 53: eight drivers 53 in the case of the LABs labelled group A, B, H, and G, and five drivers 53 in the case of the LABs labelled group C, D, F, and E. While we believe these choices to be optimum for the particular embodiment shown, other choices could be made. For example, in another embodiment (shown in FIG. 7), there are four LABs, each of which has seven tri-state drivers. In addition, the chip shown in FIG. 7 has eight dedicated inputs and four power/ground pins.

PIA blocks 60 will now be described with reference to FIG. 3. The PIA provides a mechanism for pro-

programmably routing signals from I/O input pins 40 to any LAB and from any LAB macrocell output to any other LAB. The PIA includes word lines 43 and 62 and bit lines 61. The bit lines are also labelled "interconnect terms" in FIG. 3. In the preferred embodiment shown, there are 52 word lines 43 which come from the I/O lines, and there are 128 word lines 62 which are driven from macrocell buffers 54. Interconnect terms 61 are perpendicular to the word lines. At the intersections of the word lines and bit lines are programmable elements 63 which, when programmed in one state, provide a connection between the associated word and bit lines, and which, when programmed in the other state, provide no such connection. In the preferred embodiment, the programmable elements are EPROM transistors. However, other types of programmable elements such as EEPROM transistors, fuses, anti-fuses, or other similar elements could be used. There are 24 interconnect terms 61 feeding each LAB 50 in the embodiment shown. Again, this number is an estimate as to the optimum number for the device shown in FIG. 3, but a larger or smaller number could be used if desired. The entire PIA (i.e., all of PIA blocks 60 taken together) is therefore a programmable array with 180 word lines and 192 bit lines (eight groups of 24 bit lines).

FIG. 4 is a block diagram showing a single LAB 50 and its associated PIA 60. This diagram shows, in concept, the signal routing to and from the LAB and the PIA. Lines going into the LAB are the fast inputs 570 shown as a group of  $8 \times 2 = 16$  lines (true and complement signals), the interconnect terms 580 shown as a group of  $24 \times 2 = 48$  lines (true and complement signals), the macrocell feedback lines 590 shown as two groups totaling  $16 \times 2 = 32$  lines (true and complement signals), and the "expander" feedback lines 560 shown as a group of 32 lines (single polarity only). This totals to 128 word lines for each LAB in the embodiment shown. There are 152 bit lines (P-terms) in each LAB. These will be described in detail in the discussion of FIG. 5. Shown in the diagram of FIG. 4 are the groups of signals 530 and 531 going to the output buffers labeled 53 in FIG. 3. Lines 530 provide the path for data from the macrocells to the output buffers, and lines 531 provide the path for the output enable (OE) signals from the OE P-terms. The PIA block 60 associated with this LAB is shown as having 180 word lines and 24 bit lines as previously described.

Referring now to FIG. 5, we can see more of the detail of one of the macrocells. In this case it is shown with an I/O buffer 53. If it were a buried macrocell, the only difference (at least pictorially) would be the absence of output buffer 53, the OE P-term structure (101, 103, 110), and I/O pin 40. The programmable array is shown as the intersection of word lines 102 and bit lines 101. The label 51 refers to that part labelled "macrocell" in FIG. 3, and the label 52 refers to that

part labelled "expander" in FIG. 3. Actually, in the physical layout of the chip, two expander P-terms are preferably grouped with the P-terms of each macrocell for convenience. In the description of FIG. 5, the word "macrocell" will be used to describe the entire collection of P-terms (including the two expander P-terms) and the associated logic gates 103-107, flip-flop 123, and output buffer 53, if present.

There are ten P-terms 101 in this macrocell. Each P-term receives inputs from the 128 word lines 102 (described earlier). There is a programmable element (similar to element 63 in the PIA) at the intersection of each bit line with each word line. A logical AND function of any of the word line variables can be formed by programming these elements. This is described in U.S. patent 4,617,479 and will not be repeated here. The correct logical outcome produced by each P-term is represented either as an active-low AND gate 103 or as a NOR gate 104. Those skilled in the art will recognize that other representations could be shown. For example, an active-high AND gate could be used if one notes that the opposite polarity word line were used as its input and thus achieve the same logical result.

The purpose of each P-term is as follows: The P-term labelled OE is used as the output enable for the associated output buffer 53. If this were a buried macrocell, this bit line would be absent. SETN is used to control the preset of flip-flop 123. The next three terms, P0, P1, and P2, feed OR gate 105 which produces a logical sum-of-products at its output 115. This collection of P-terms, in conjunction with gate 105, forms the "programmable AND, fixed OR" function described in U.S. patent 4,124,899. The term labeled INV is used as an "invert control" for XOR gate 107. This allows for the creation of inverted sum-of-product functions at line 121. This will be recognized by those skilled in the art as expanding the number of possible functions which can be realized. In addition to acting as a static control for the inverted sum-of-products option, the INV term can be used "dynamically" as a direct input to the XOR gate 107. For example, any logic function which can be reduced to (1) an EXCLUSIVE-OR of an AND function with an AND-OR function, (2) an EXCLUSIVE-OR of an OR function with an OR-AND function, (3) an EXCLUSIVE-OR of an OR function with an AND-OR function, or (4) an EXCLUSIVE-OR of an AND function with an OR-AND function can be implemented directly in one pass through the array. (This is shown in detail in FIGS. 8a and 8c; the dollar sign in FIG. 8a represents the EXCLUSIVE-OR function.) ACLK is used to create an "asynchronous" clock signal for flip-flop 123 in conjunction with gate 106 and gates 109 and 108. CLEARN is used to control the "Clear" line on flip-flop 123. EXP1 and EXP2 are the "expander" P-terms. Note that each expander 52 preferably includes only a single P-term.

Our assignee has studied the most often used logic functions in relation to a variety of possible architectures. In particular, the AND-OR-XOR structure of P0, P1, P2, OR gate 105, and XOR gate 107 was analyzed assuming both less than three AND P-terms (e.g., two AND P-terms) feeding OR gate 105, and more than three AND P-terms (up to eight P-terms such as is used in the prior art macrocell of FIG. 2) feeding the OR gate. The classes of functions included the following: adders, comparators, counters, decoders, demultiplexers, parity generators, and shift registers. The purpose of the study was to evaluate the architecture of the present invention relative to the prior art architecture of FIG. 2. The present new architecture is a combination of three programmable ANDs, a fixed OR, and an XOR, with single-P-term "expanders". This architecture is believed to be superior to both the prior art structure shown in FIG. 2 and to the single-P-term architectures proposed in the above-mentioned Goetting et al. reference. The study bore this out and reached several other important conclusions. It was found that having less than three P-terms feeding the OR gate is very restrictive when doing counters and shift registers. For all other functions examined, three P-terms feeding the OR gate was always as good as four P-terms feeding the OR. (This is only true assuming that in either case there is the additional BLIV P-term and XOR gate 107.) The prior art eight-P-term architecture is only superior for a very limited group of functions (for example, multiplexers with more than four inputs). The study also demonstrated that having approximately two expander P-terms per macrocell was more than sufficient to accommodate the less common functions which require many P-terms.

Expanders 52 play an important role in this new architecture. As their name implies, these P-terms allow for growth. That is, they allow for implementation of those (less common) functions which do not fit within the three-P-term limit (for example, an 8-to-1 multiplexer can be fit into 9 expanders). Expander P-terms anywhere in the LAB can be used to form elements of these more complex functions, and then the outputs of these P-terms are combined using another P-term (typically one of the P-terms feeding a fixed OR gate 105) (see, for example, FIG. 8f). Functions formed with expander P-terms can also be used to feed other expanders on single P-terms such as INV, ACLK, SETN, CLEARN, or OE. Also, there are often common P-terms which can be used by a number of logic functions. These common P-terms can be formed by the expanders and then fed to those functions (which are likely to be implemented in a programmable AND, fixed OR section) for which they are required. FIG. 8e shows an example of a logic expression which requires more than three P-terms which can be factored into expressions which can be formed using the expander P-terms and recombined using

another P-term (typically this will be a P-term which feeds the fixed OR gate). In FIG. 8e, the original expression has been factored such that two factors are implemented in two expanders and then combined with the remainder of the expression in one of the P-terms feeding the fixed OR gate. The original expression was:

$$\begin{aligned} \text{FUNCTION} = & A * D * X * Y + A * E * X * Y + \\ & B * D * X * Y + B * E * X * Y + C * D * X * Y + \\ & C * E * X * Y \end{aligned}$$

This expression can be factored and rewritten as:

$$\text{FUNCTION} = (X * Y) * (A + B + C) * (D + E)$$

The common factors  $X*Y$  are formed on the P-term feeding the fixed OR gate, while the remaining factors  $(A+B+C)$  and  $(D+E)$  are formed on each of two expanders and fed to the P-term which contains the  $X*Y$  term. In this example, an expression which would have required six P-terms to implement can now be done in three P-terms. Suppose further that either the expression  $(A+B+C)$  or the expression  $(D+E)$  were required by some other macrocell or macrocells. These same expressions formed on the expander P-terms could be used again by those other macrocells. Thus an expression generated on the expanders can be amortized across all of the macrocells which have the expanders' outputs as word line inputs. This again results in an overall saving of valuable P-term resources. Examples of various types of logic functions which can be fit into the P-term structure of the present invention are shown in FIGS. 8a through 8g. Latches require only two expanders. This structure is shown in FIG. 8h.

Continuing now with FIG. 5, XOR gate 107 receives its inputs from OR gate 105 and P-term INV. Those skilled in the art will recognize that if the logic signal on line 116 is 0, then the output of XOR gate 107 (line 121) will have the same logic value as input 115. On the other hand if line 116 is 1, then 121 will be the logical inversion of 115. In addition to allowing for inverted sum-of-product functions, or positive or inverted product-of-sum functions, this structure, in conjunction with a D flip-flop such as 123, also allows for emulating other flip-flop types such as T, J-K, and R-S. Emulation of various flip-flop types using array logic and XOR gates is the subject of U.S. patent 4,677,318. When using the expander P-terms as an AND array and the P-terms feeding the OR gate 105 as an OR array, the INV signal 116 needs to be set to a logic 1.

Flip-flop block 123 appears to be a simple D flip-flop with active low preset (P) and clear (C). However, this is done for simplicity of illustration of the macrocell. FIG. 9 is a truth table which explains the full functionality of element 123. Note that if  $P = C = 1$ , then 123 is an edge-triggered flip-flop. At the rising edge of CLK (line 122 in FIG. 5), whatever data is present at the D input 121 is transferred to the Q output 124. If P is 0 and C is 1, then the Q output will be forced to

1 independent of the state of CLK or D. If C is 0 and P is 1, then the Q output will be forced to 0 independent of the state of CLK or D. To those skilled in the art, the case where  $P = C = 0$  is an illegal condition and is not defined. For flip-flop 123, however, when  $P = C = 0$ , the flip-flop is redefined as shown in FIG. 9. It thus becomes a "flow-through latch". Then, whenever line 122 is high, the Q output takes the value of whatever is on the D input. Whenever line 122 is low, the Q output holds the value that was present at the D input when line 122 went low. If line 122 is held high (for example, by programming P-term ACLK high), then signals will propagate directly from 121 to 124. This is the same "combinatorial" function as was provided by multiplexers and architectural control EPROM bits on prior art EPLD circuits. The present new design is simpler, faster, and provides greater functionality. As has been mentioned, a preferred structure for implementing flip-flop 123 is shown in US-A-4 864 161.

The output signal 124 from flip-flop 123 (1) goes to the input of output driver 53, (2) feeds back (via buffer 54) to a word line driver 57 of its own LAB, and (3) drives one of the word lines of the PIA (indicated as line 62 in FIG. 3). This signal 124 can be used by any other LAB via its connection through the PIA. The signal also feeds a conventional tri-state I/O buffer 53 such that if the buffer is enabled by line 110, the signal from 124 will drive off chip through I/O pin 40. I/O pin 40 can also provide an input path from off chip via line 41. This line drives buffer 42 (FIG. 3) whose output becomes one of the word lines for the PIA shown as line 43 in FIG. 3. I/O buffer 53 can be dynamically controlled by the OE P-term, in which case pin 40 may be both an input and an output depending upon the state of line 110. Alternatively, by programming the chip such that OE is always 0, buffer 53 will always be disabled, in which case I/O pin 40 can be used permanently as an input. Thus each of I/O pins 40 can be configured as input, output, or bi-directional input/output terminals. Because of the feedback of signal 124 to the LAB and the PIA, and the I/O input line 41, disabling of the output driver 53 does not result in the loss of the macrocell's functionality. This is a significant advantage over some prior art devices.

Turning now to the clock structure for the LAB, this structure includes inverter 109, AND gate 108, OR gate 106, and P-term ACLK. Three modes of operation are anticipated as follows:

**COMBINATORIAL MODE:** In this case,  $P = C = 0$  as previously described. Further, the ACLK P-term is programmed to always be 1, and line 122 is therefore also always 1. Whatever data is present at line 121 will pass through flip-flop 123 and appear at line 124.

**ASYNCHRONOUS MODE:** In this case, the line labeled ECKN (which is an extra P-term (not shown) in the LAB) is programmed to be 1. This means that line 125 is logic 0. Then line 122 is directly controlled

by the state of the ACLK P-term. ACLK can be any (inputs active-low) AND function of any of the word line variables. Each flip-flop in the LAB has its own separate ("asynchronous") P-term clock.

**SYNCHRONOUS MODE:** P-term ACLK is programmed to be always 0. Also, ECKN is programmed to be 0 and thus ECK is 1. This allows the signal EXT.(SYNC.) CLK. on line 32 to propagate through AND gate 108 and appear on line 125. EXT.(SYNC.) CLK. line 32 comes from an input pad (one of the "fast inputs") not shown. This signal on line 125 passes through OR gate 106 and appears on line 122. In this way, an external signal can directly control the clocking of flip-flop 123. Because there is a single ECKN P-term per LAB, the selection of synchronous mode is done on a per LAB basis rather than on a per macrocell basis.

Another advantage of the chip architecture of the present invention is that chips of any given configuration can be packaged in any of a variety of ways with no loss of internal resources. For example, FIG. 6a illustrates one way in which the chip of FIG. 3 can be bonded out to 68 pins, while FIG. 6b shows how the same chip can be bonded out to 40 pins. The chip pads which are not bonded out in FIG. 6b are certain I/O pins. However, the "output" signals that could be applied to these chip pads are still usable internally, and the remaining external inputs can be applied to any LAB via PIA 60. Thus, even though some chip pads are not bonded out in FIG. 6b, the only loss in chip capability is the loss of the external chip I/O connections. (With reference to FIGS. 6a and 6b, the eight LABs on the chip are designated A through H. Thus, for example, in FIG. 6a eight I/O pads I/OA0-8 of LAB A are bonded out to lead tips 11 through 4, respectively, while in FIG. 6b only four I/O pads I/OA0, 1, 2, and 7 are bonded out to lead tips 37 through 34, respectively. In FIG. 6a LABs A, D, E, and H each have eight bonded-out I/O pads and the remaining LABs each have five bonded-out I/O pads. In FIG. 6b LABs A, D, E, and H each have four bonded-out I/O pads and the remaining I/O pads each have three bonded out I/O pads. In both FIG. 6a and 6b the "fast" inputs are designated I0 through I7.)

Although particular numbers of such components as macrocells, expanders, fast inputs, and array inputs from the PIA are employed in the depicted embodiments described above, it will be understood that (among other possible variations within the scope of the invention that will occur to those skilled in the art) any number of such components can be used without departing from the scope of the invention as defined by the appended claims.

## Claims

1. A programmable logic device (10) including first



(A) and second (B or C or D or E or F or G or H) logic array blocks, each including a plurality of word line conductors (102), a plurality of P-term line conductors (101) each of which is programmably interconnectable to at least some of said word line conductors (102) for producing on each P-term line conductor (101) a signal which is a logical function of the signals on the word line conductors (102), and means (eg 103, 104, 107, 123) for deriving output signals (124) from at least one of said P-term line conductor (101) signals of at least said first logic array block, a programmable interconnect array (60) being provided for selectively applying said output signals (124) to any of a plurality of the word line conductors (102) of the second of said logic array blocks (eg, B or C or D or E or F or G) characterised in that said programmable interconnect array (60) comprises a plurality of word lines (62) each of which receives a respective one of said output signals (124), a plurality of bit lines (61) perpendicular to said word lines (62), each of which bit lines is connected to a respective one of said plurality of the word line conductors (102) of said second of said logic array blocks (eg, B or C or D or E or F or G), and programmable elements (63) at the intersection of said word lines and bit lines for selectively programmably connecting each of said bit lines (61) to any one of said word lines (62).

2. The device defined in Claim 1, in which means (57) is provided for applying the output signal (124) of at least one logic array block (A) to at least one of the word line conductors (102) of said at least one logic array block (A).
3. The device defined in Claim 1, in which at least one of said P-term line conductor signals (119 or 120) in at least one of said logic array blocks (A) is applied to at least one of the word line conductors (102) of that logic array block (A).
4. The device defined in Claim 1, in which at least one of said P-term line conductor signals (119 or 120) in at least one of said logic array blocks (A) is applied only to one of the word line conductors (102) of that logic array block (A).
5. The device defined in Claim 1, including means (40) for receiving an input signal (41) applied to the programmable logic device (10), in which the programmable interconnect array (60) selectively applies said input signal (41) to any of a plurality of the word line conductors (102) of at least one of said logic array blocks (A).
6. The device defined in Claim 5, in which the programmable interconnect array (60) selectively

applies said input signal (41) to any of a plurality of the word line conductors (102) in either or both of said first (A) and second (B or C or D or E or F or G or H) logic array blocks.

7. The device defined in Claim 1, in which said programmable interconnect array (60) also selectively applies the output signals (124) of the other of said logic array block (eg B or C or D or E or F or G) to any of a plurality of the word line conductors (102) of said at least some logic array blocks (eg A or H).

## Patentansprüche

1. Programmierbare Logikvorrichtung (10) mit einem ersten (A) und einem zweiten (B oder C oder D oder E oder F oder G oder H) Logikgatterblock, von denen jeder mehrere Wortleiter (102), mehrere P-Term-Leiter (101), von denen jeder programmierbar an mindestens einige der Wortleiter (102) zum Erzeugen eines Signals auf jedem P-Term-Leiter (101) schaltbar ist, das eine logische Funktion des Signals auf dem Wortleiter (102) ist, und eine Einrichtung (z.B. 103, 104, 107, 123) zum Ableiten von Ausgangssignalen (124) von mindestens einem der Signale der P-Term-Leiter (101) von mindestens dem ersten Logikgatterblock aufweist, wobei ein programmierbares Schaltgatter (60) zum selektiven Übertragen der Ausgangssignale (124) an irgend einen der mehreren Wortleiter (102) des zweiten Logikgatterblocks (z.B. B oder C oder D oder E oder F oder G) vorgesehen ist, dadurch gekennzeichnet, daß das programmierbare Schaltgatter (60) mehrere Wortleitungen (62), von denen jeder ein entsprechendes der Ausgangssignale (124) empfängt, mehrere senkrecht zu den Wortleitungen (62) angeordnete Bitleitungen (61), wobei jede der Bitleitungen mit einem entsprechenden der mehreren Wortleiter (102) des zweiten Logikgatterblocks (z.B. B oder C oder D oder E oder F oder G) verbunden ist, und programmierbare Elemente (63) an der Kreuzung der Wortleitungen und Bitleitungen zum selektiven programmierbaren Verbinden jeder der Bitleitungen (61) mit irgendeiner der Wortleitungen (62) aufweist.
2. Vorrichtung nach Anspruch 1, wobei eine Einrichtung (57) zum Übertragen des Ausgangssignals (124) von mindestens einem Logikgatterblock (A) an mindestens einen der Wortleiter (102) von mindestens einem Logikgatterblock (A) vorgesehen ist.
3. Vorrichtung nach Anspruch 1, wobei mindestens eines der Signale (119 oder 120) der P-Term-Lei-

ter in mindestens einem der Logikgatterblöcke (A) an mindestens einen der Wortleiter (102) des Logikgatterblocks (A) übertragen wird.

4. Vorrichtung nach Anspruch 1, wobei mindestens eines der Signale (190 oder 120) der P-Term-Leiter in mindestens einem der Logikgatterblöcke (A) an nur einen der Wortleiter (102) dieses Logikgatterblocks (A) übertragen wird.
5. Vorrichtung nach Anspruch 1 mit einer Einrichtung (40) zum Empfangen eines Eingangssignals (41), das an die programmierbare Logikvorrichtung (10) übertragen wird, wobei das programmierbare Schaltgatter (60) selektiv das Eingangssignal (41) an irgend eines von mehreren der Wortleiter (102) von mindestens einem der Logikgatterblöcke (A) überträgt.
6. Vorrichtung nach Anspruch 5, wobei das programmierbare Schaltgatter (60) selektiv das Eingangssignal (41) an irgend eines von mehreren der Wortleiter (102) in einem oder in beiden der ersten (A) und zweiten (B oder C oder D oder E oder F oder G oder H) Logikgatterblöcke überträgt.
7. Vorrichtung nach Anspruch 1, wobei das programmierbare Schaltgatter (60) ebenso selektiv die Ausgangssignale (124) vom anderen Logikgatterblock (z.B. B oder C oder D oder E oder F oder G) an irgend einen von mehreren Wortleitern (102) von mindestens einigen Logikgatterblöcken (z.B. A oder H) überträgt.

#### Revendications

1. Dispositif logique programmable (10) comprenant des premiers (A) et des seconds (B ou C ou D ou E ou F ou G ou H) blocs de matrices logiques, comprenant chacun une pluralité de lignes conductrices de mots (102), une pluralité de lignes conductrices de termes P (101), dont chacune peut être interconnectée de façon programmée avec au moins certaines desdites lignes conductrices de mots (102) pour produire sur chaque ligne conductrice de termes P (101) un signal qui est une fonction logique des signaux sur les lignes conductrices de mots (102), et des moyens (par exemple 103, 104, 107, 123) pour dériver des signaux de sortie (124) de l'un au moins desdits signaux d'au moins ledit premier bloc de matrices logique de ladite ligne conductrice de termes P (101), une matrice d'interconnexion programmable (60) étant prévue pour appliquer sélectivement lesdits signaux de sortie (124) à l'une quelconque d'une pluralité de lignes

conductrices de mots (102) des seconds desdits blocs de matrices logiques (par exemple B ou C ou D ou E ou F ou G), caractérisé en ce que ladite matrice d'interconnexion programmable (60) comprend une pluralité de lignes conductrices de mots (62) dont chacune reçoit l'un desdits signaux de sortie respectifs (124), une pluralité de lignes de bits (61) perpendiculaires auxdites lignes de mots (62), chacune desdites lignes de bits étant reliée à l'une de ladite pluralité de lignes conductrices de mots respectives (102) desdits seconds blocs de matrices logiques (par exemple B ou C ou D ou E ou F ou G), et des éléments programmables (63) à l'intersection entre lesdites lignes de mots et lesdites lignes de bits pour relier sélectivement de façon programmable chacune desdites lignes de bits (61) avec l'une quelconque desdites lignes de mots (62).

2. Dispositif selon la revendication 1, dans lequel des moyens (57) sont prévus pour appliquer le signal de sortie (124) d'au moins un bloc de matrices logiques (A) à au moins l'une des lignes conductrices de mots (102) dudit au moins un bloc de matrices logiques (A).
3. Dispositif selon la revendication 1, dans lequel l'un au moins desdits signaux (119 ou 120) des lignes conductrices de termes P dans au moins l'un desdits blocs de matrices logiques (A) est appliqué à au moins l'une des lignes conductrices de mots (102) de ce bloc de matrices logiques (A).
4. Dispositif selon la revendication 1, dans lequel au moins l'un desdits signaux (119 ou 120) des lignes conductrices de termes P dans au moins l'un desdits blocs de matrices logiques (A) est appliqué seulement à l'une des lignes conductrices de mots (102) de ce bloc de matrices logiques (A).
5. Dispositif selon la revendication 1, comprenant des moyens (40) pour recevoir un signal d'entrée (41) appliqué au dispositif logique programmable (10), dans lequel la matrice d'interconnexion programmable (60) applique sélectivement ledit signal d'entrée (41) à l'une quelconque d'une pluralité de lignes conductrices de mots (102) de l'un au moins desdits blocs de matrices logiques (A).
6. Dispositif selon la revendication 5, dans lequel la matrice d'interconnexion programmable (60) applique sélectivement ledit signal d'entrée (41) à l'une quelconque d'une pluralité de lignes conductrices de mots (102) dans l'un quelconque ou les deux desdits premiers (A) et seconds (B ou C ou D ou E ou F ou G ou H) blocs de matrices

logiques.

7. Dispositif selon la revendication 1, dans lequel ladite matrice d'interconnexion programmable (60) applique également sélectivement les signaux de sortie (124) de l'autre desdits blocs de matrices logiques (par exemple B ou C ou D ou E ou F ou G) à l'une quelconque d'une pluralité de lignes conductrices de mots (102) de certains au moins desdits blocs de matrices logiques (par exemple A ou H).

5

10

15

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25

30

35

40

45

50

55

11

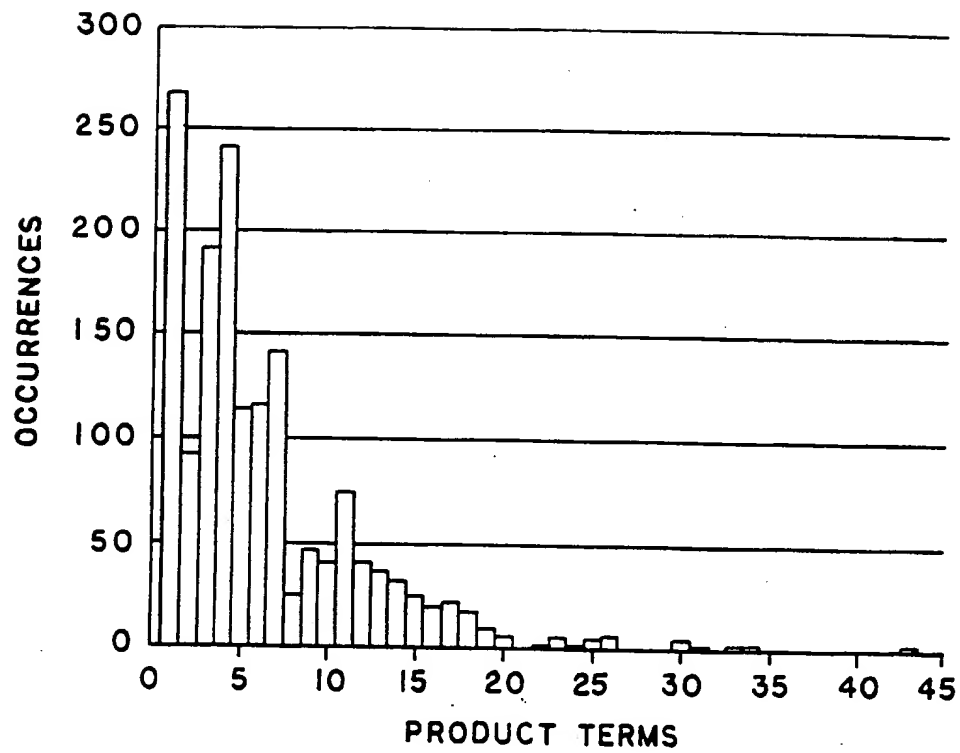
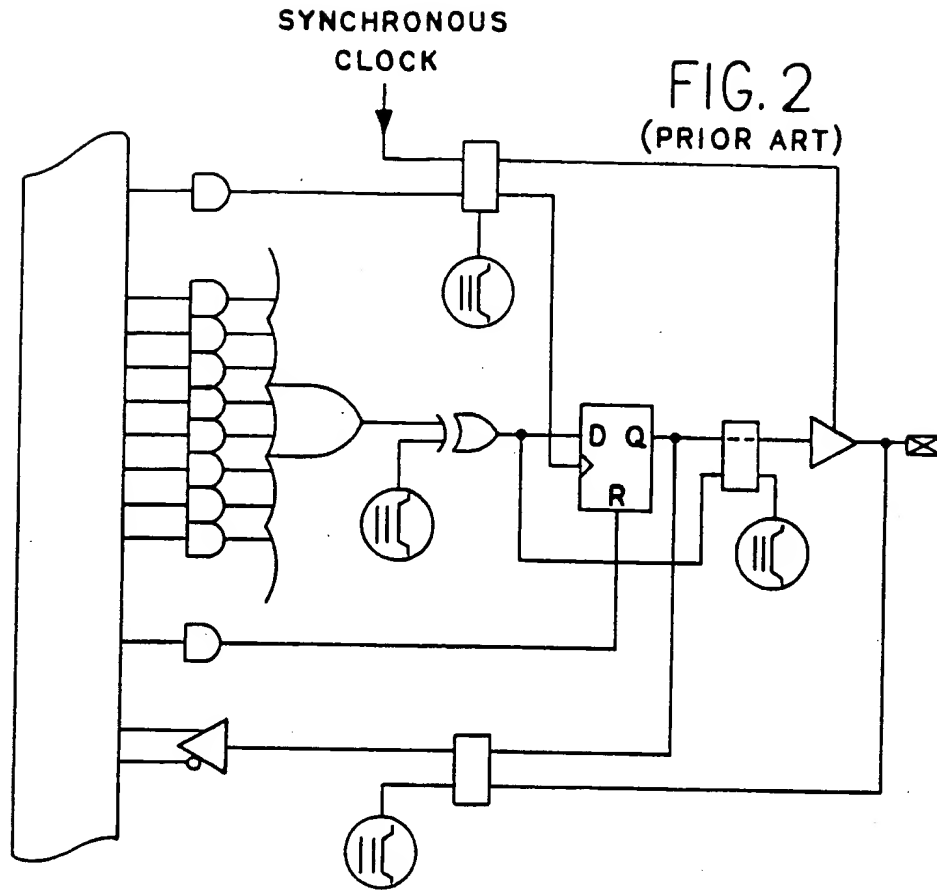
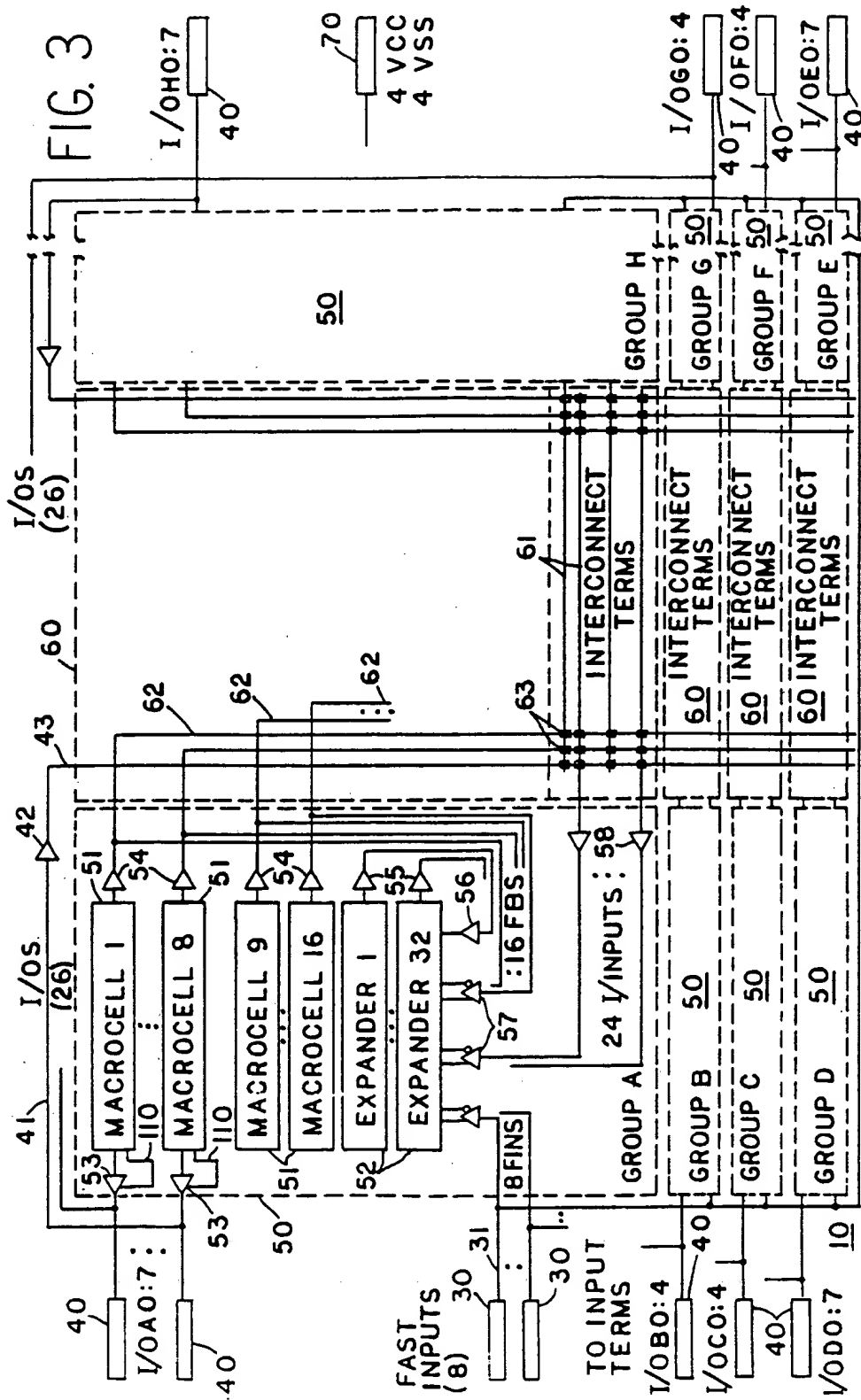


FIG.1



P	C	D	CLK	Q
1	1	0		0
1	1	1		1
1	0	X	X	0
0	1	X	X	1
0	0	X	0	Q <sub>0</sub>
0	0	0	1	0
0	0	1	1	1

FIG. 9



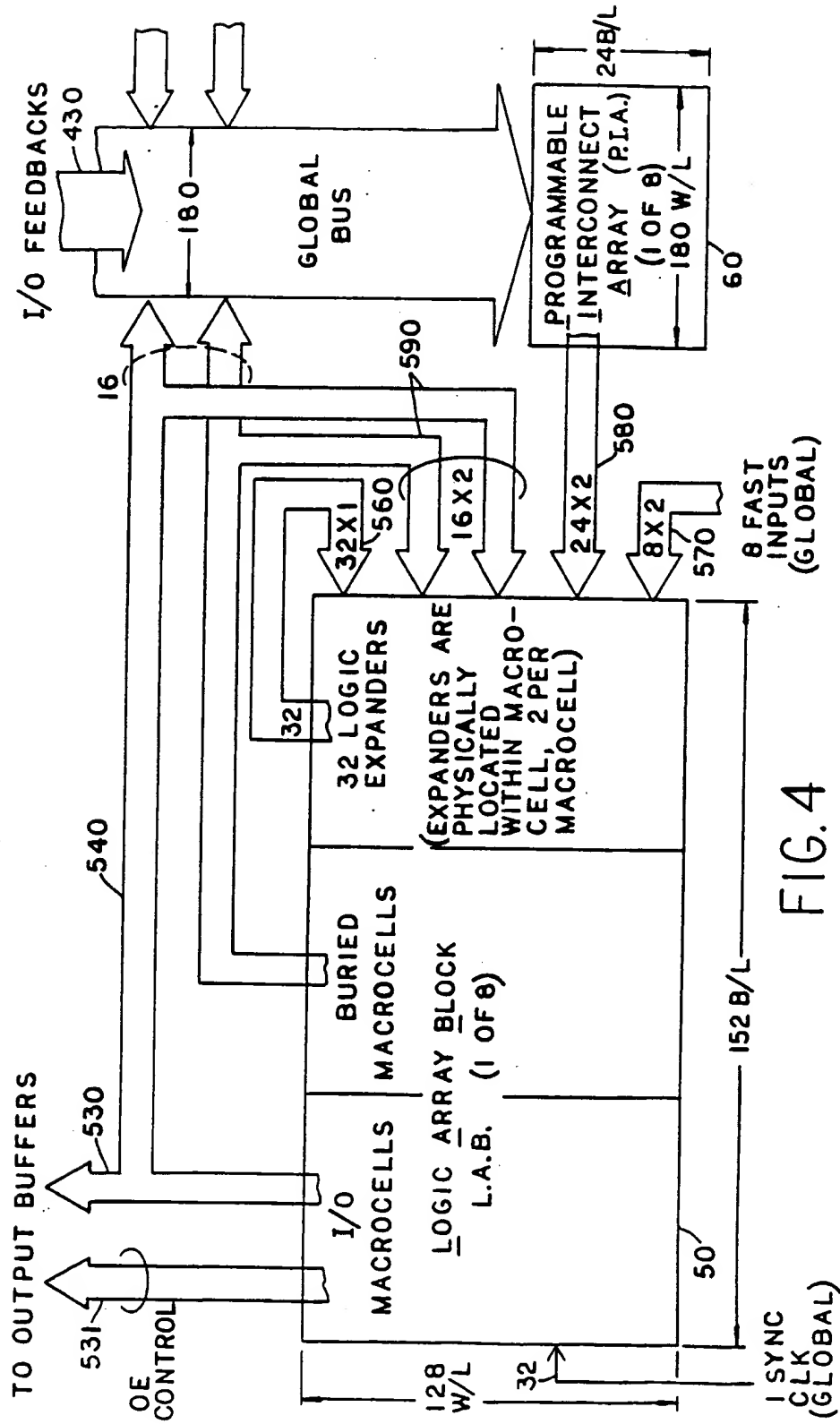


FIG. 4

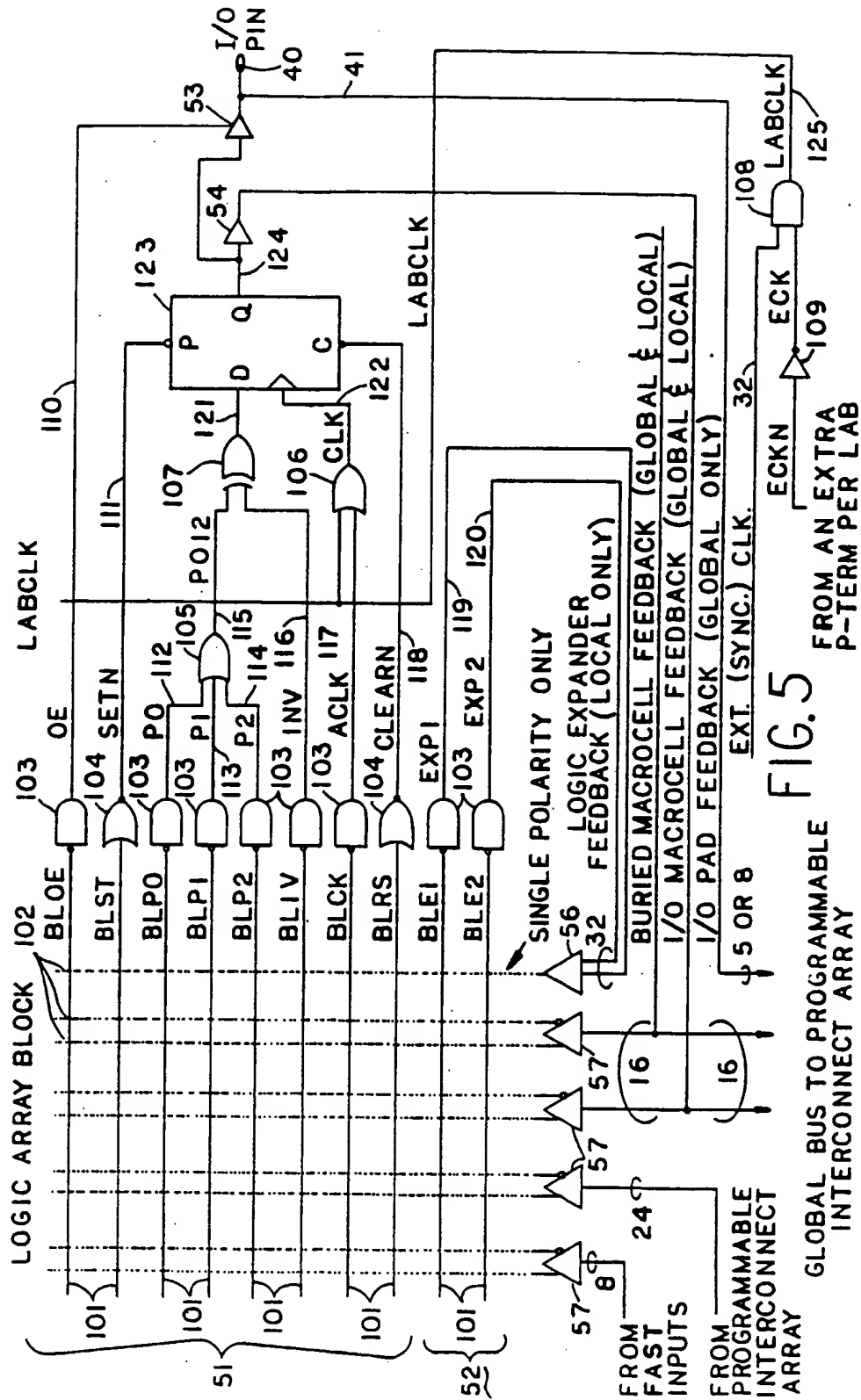


FIG. 5

GLOBAL BUS TO PROGRAMMABLE INTERCONNECT ARRAY



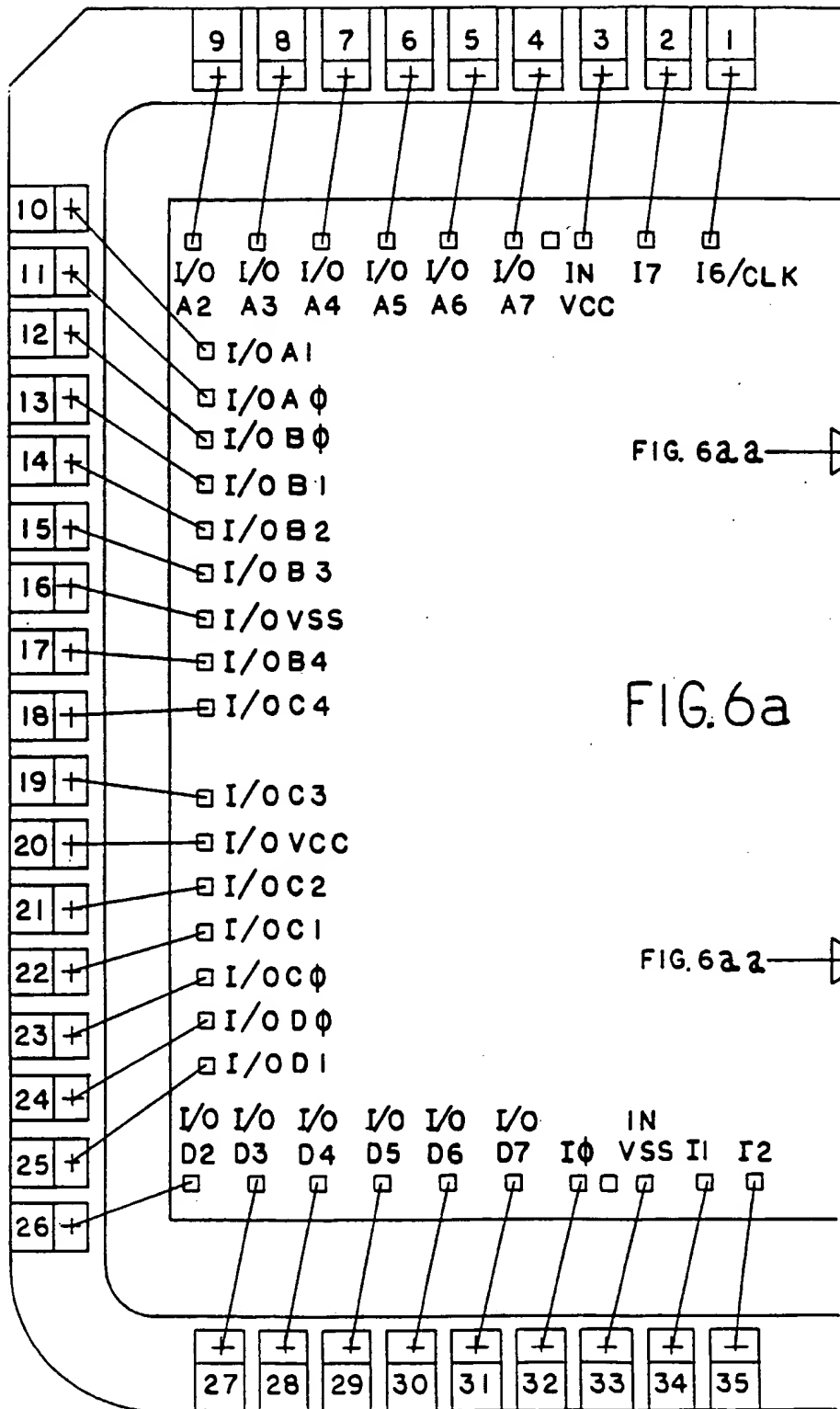
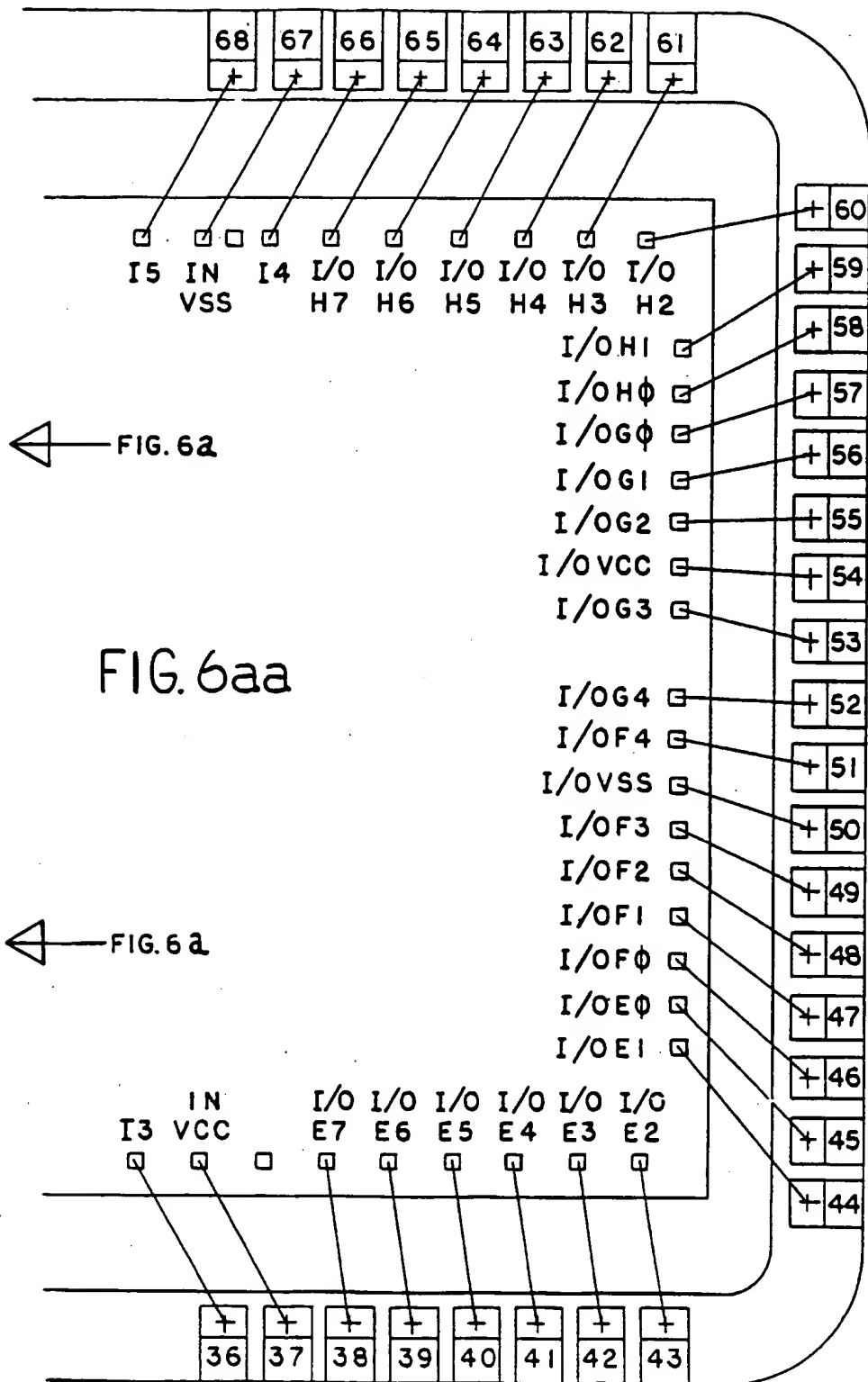
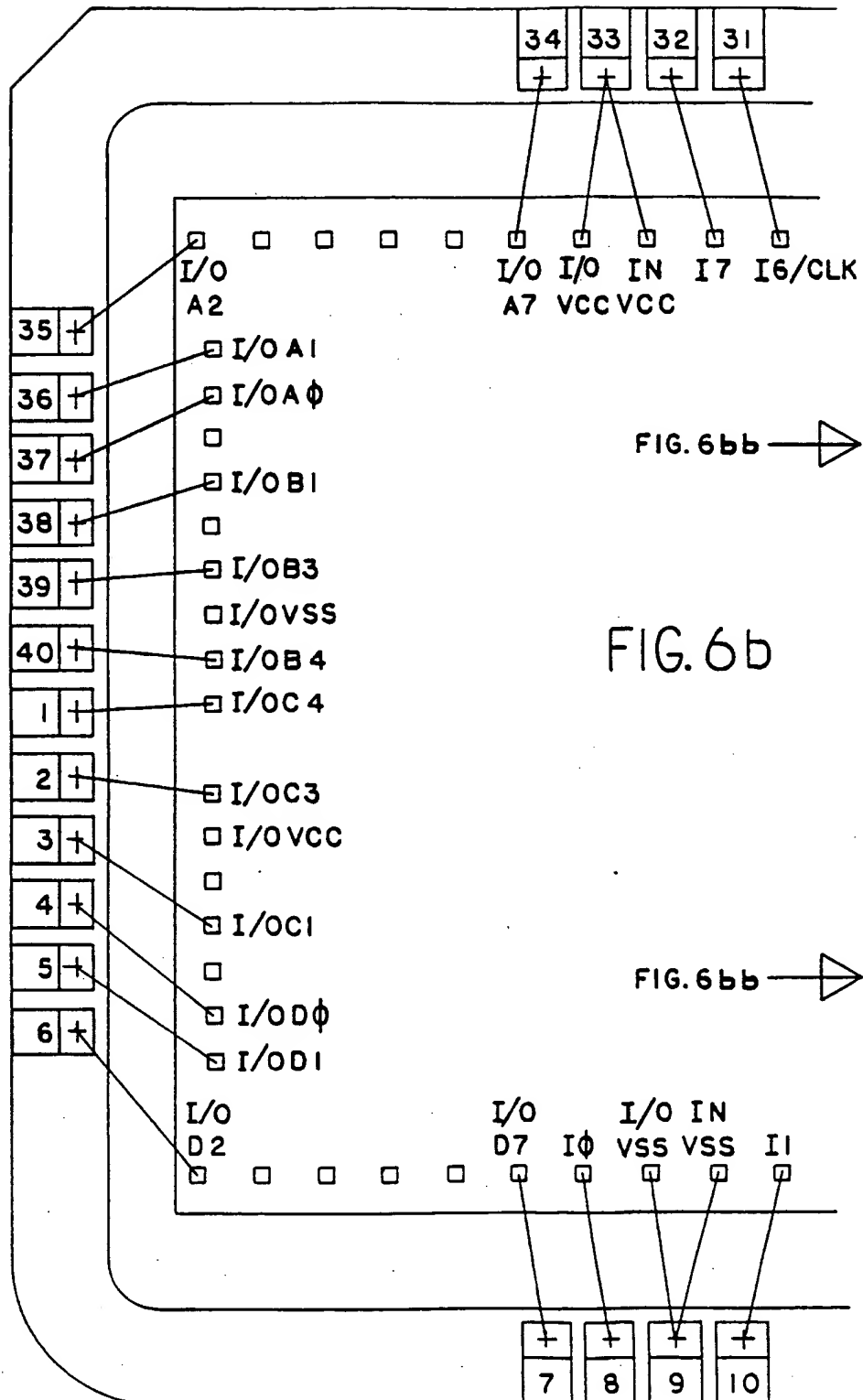


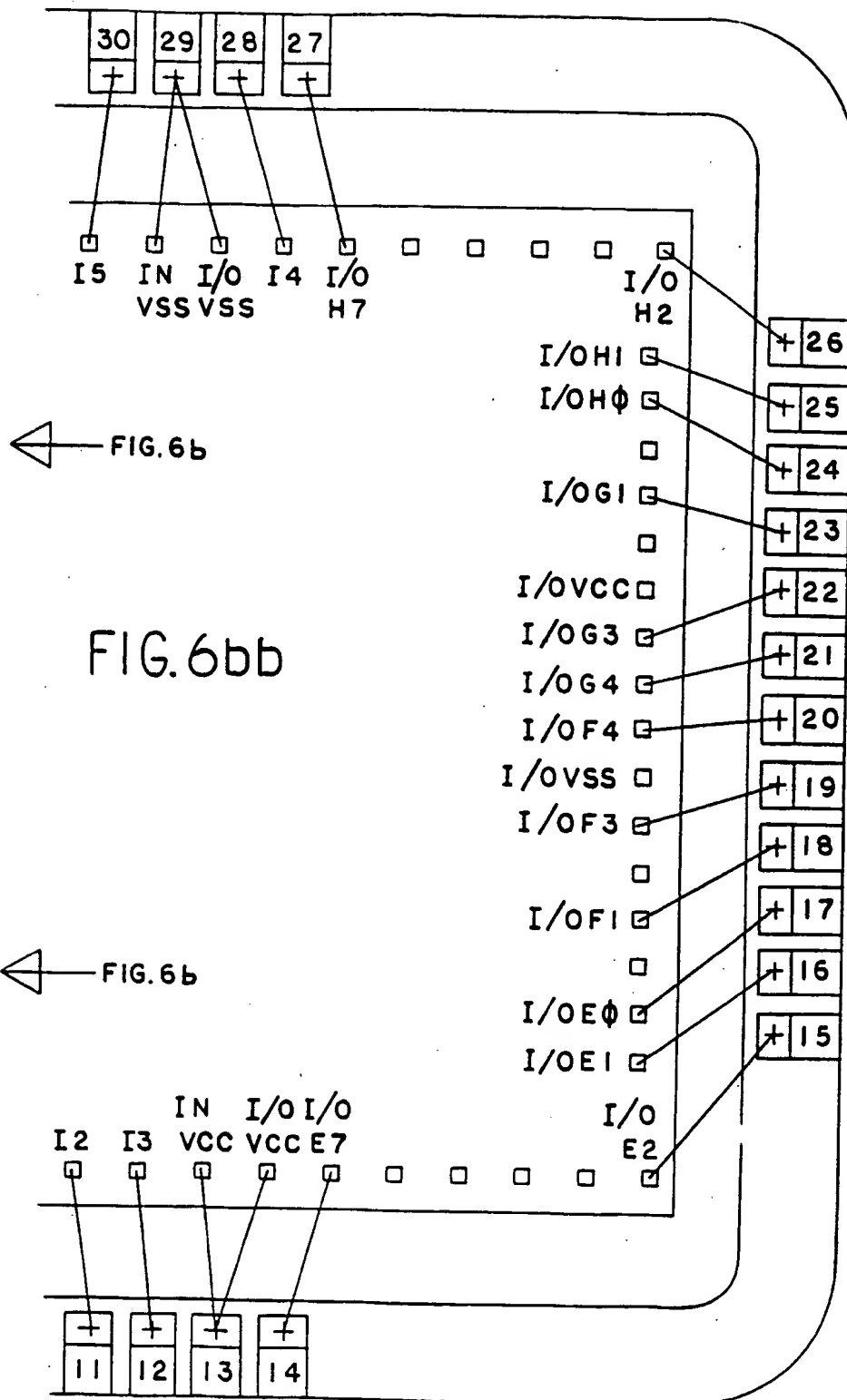
FIG. 6a.2 →

FIG. 6a

FIG. 6a.2 →







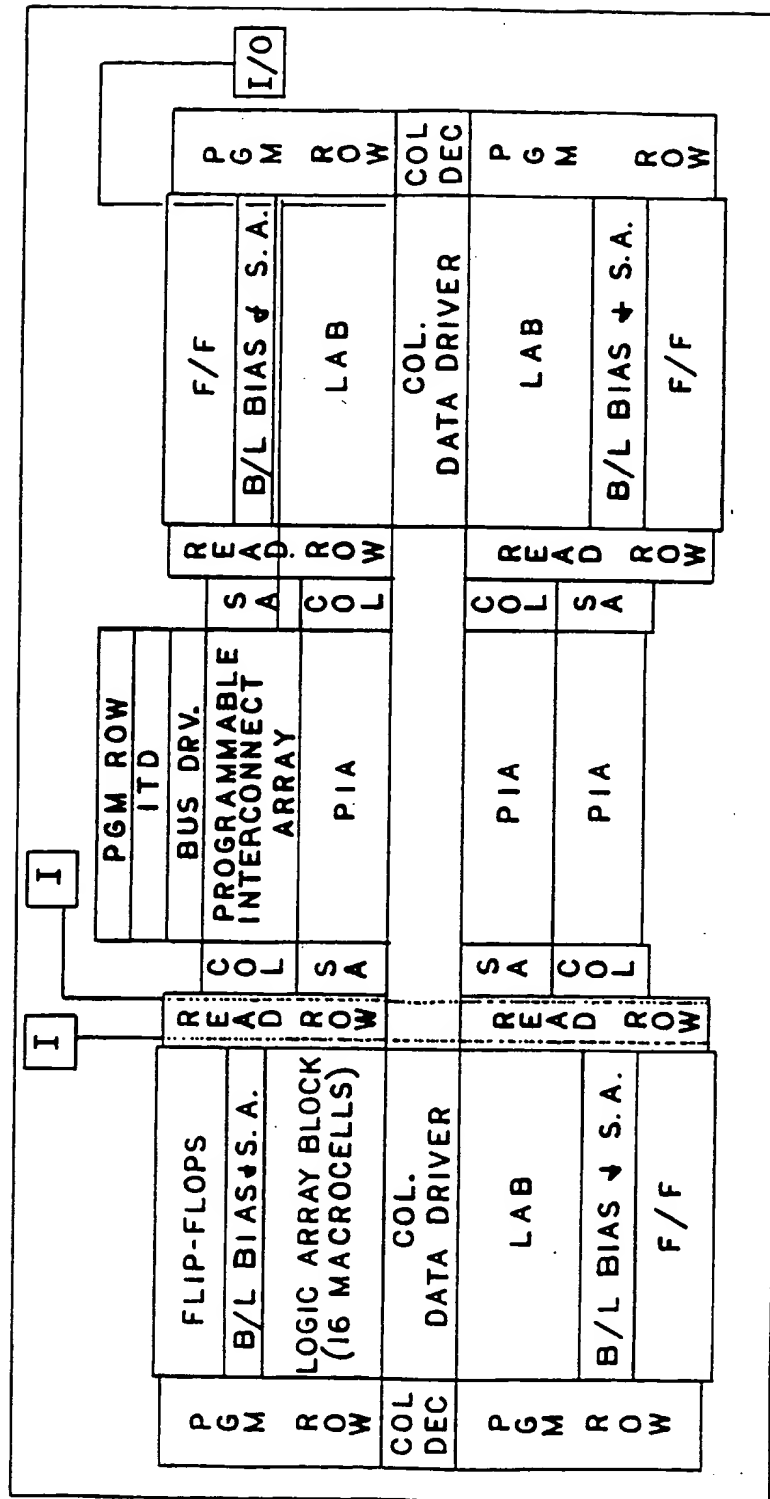
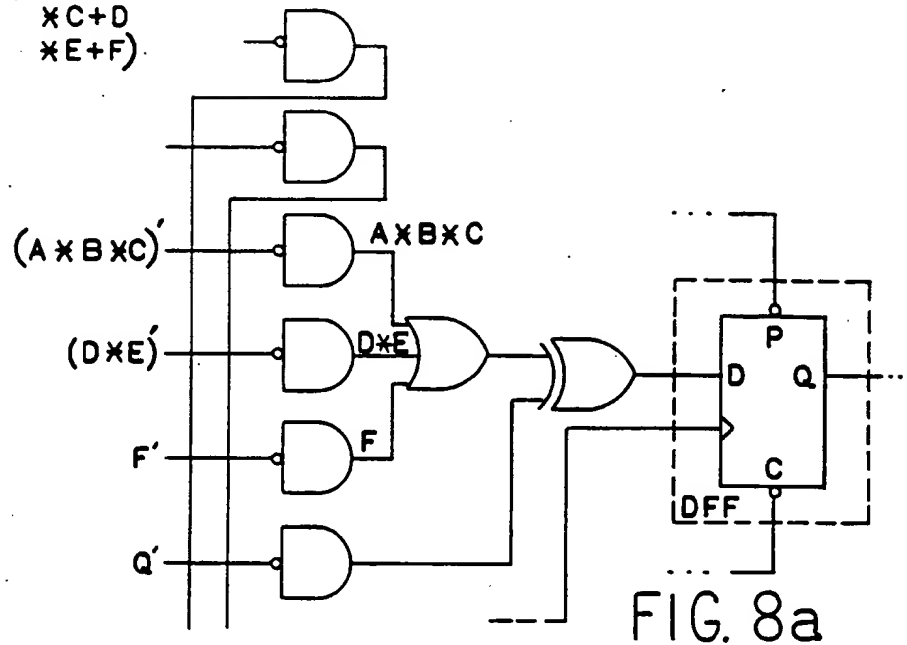
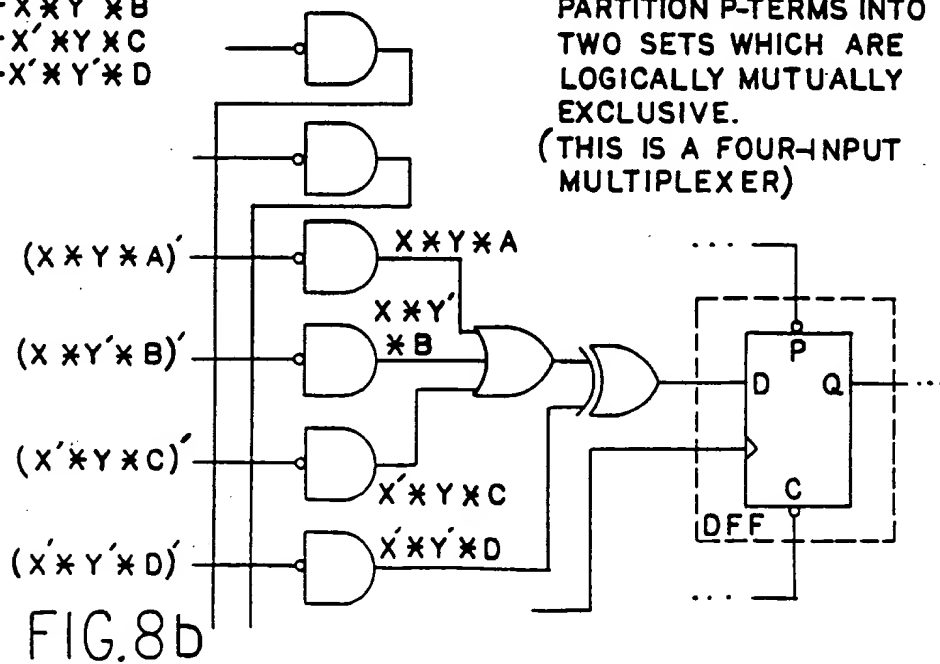


FIG. 7

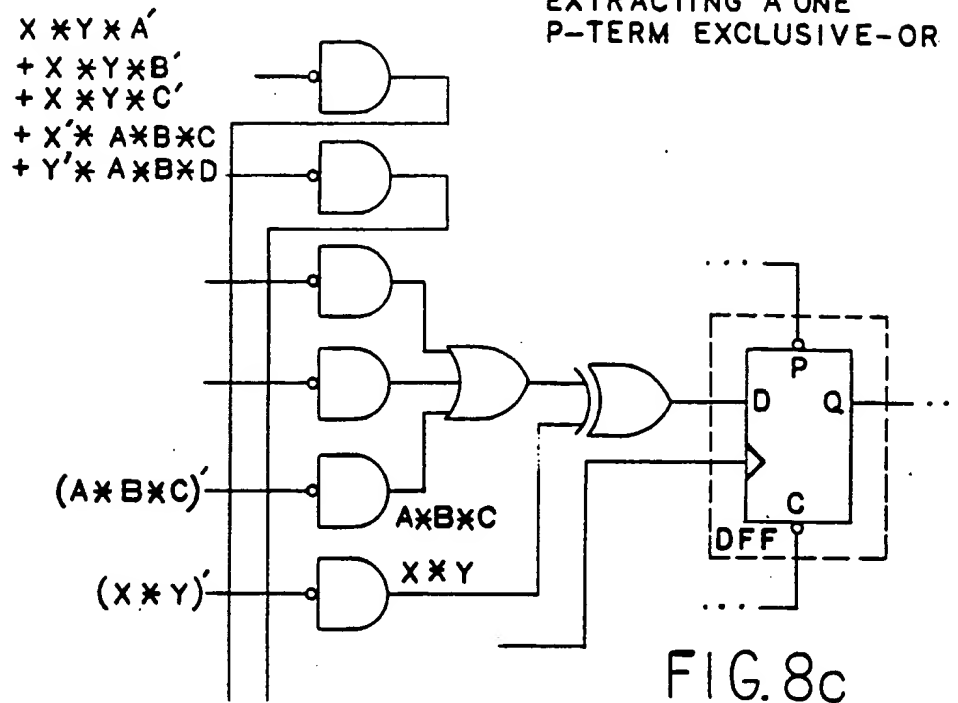
ORIGINAL:      SYNTHESIZED AS:

$$Q \text{ } \$ (A \times B \\ \times C + D \\ \times E + F)$$
FINDING AN XOR IN THE  
USER'S DESIGN

ORIGINAL:      SYNTHESIZED AS:

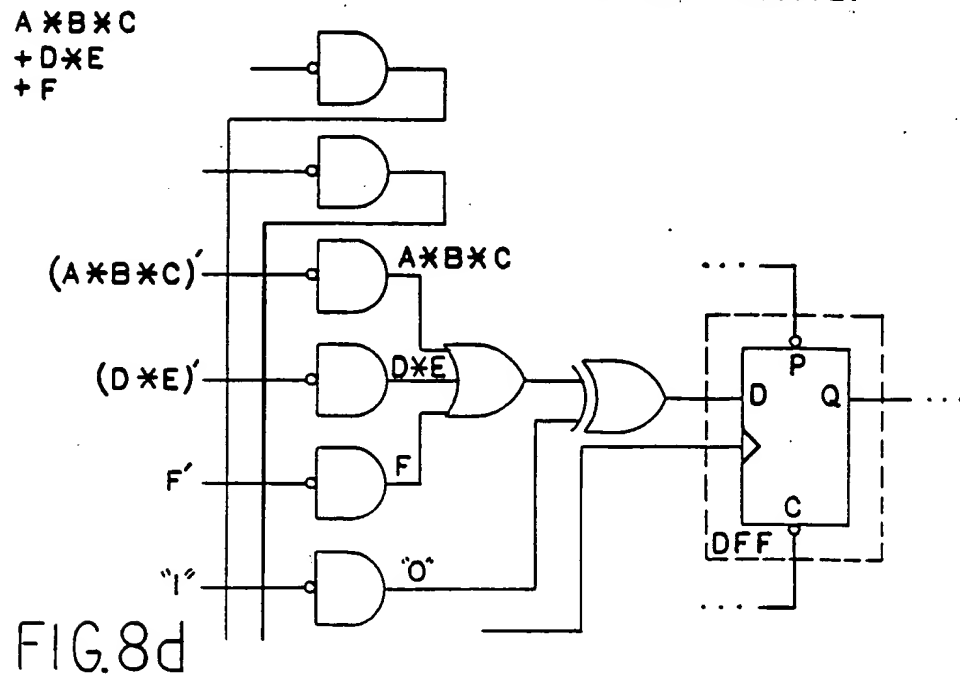
$$X \times Y \times A \\ + X \times Y' \times B \\ + X' \times Y \times C \\ + X' \times Y' \times D$$
FINDING COSETS TO GO  
ON THE XOR.  
PARTITION P-TERMS INTO  
TWO SETS WHICH ARE  
LOGICALLY MUTUALLY  
EXCLUSIVE.  
(THIS IS A FOUR-INPUT  
MULTIPLEXER)

ORIGINAL: SYNTHESIZED AS:

EXTRACTING A ONE  
P-TERM EXCLUSIVE-OR

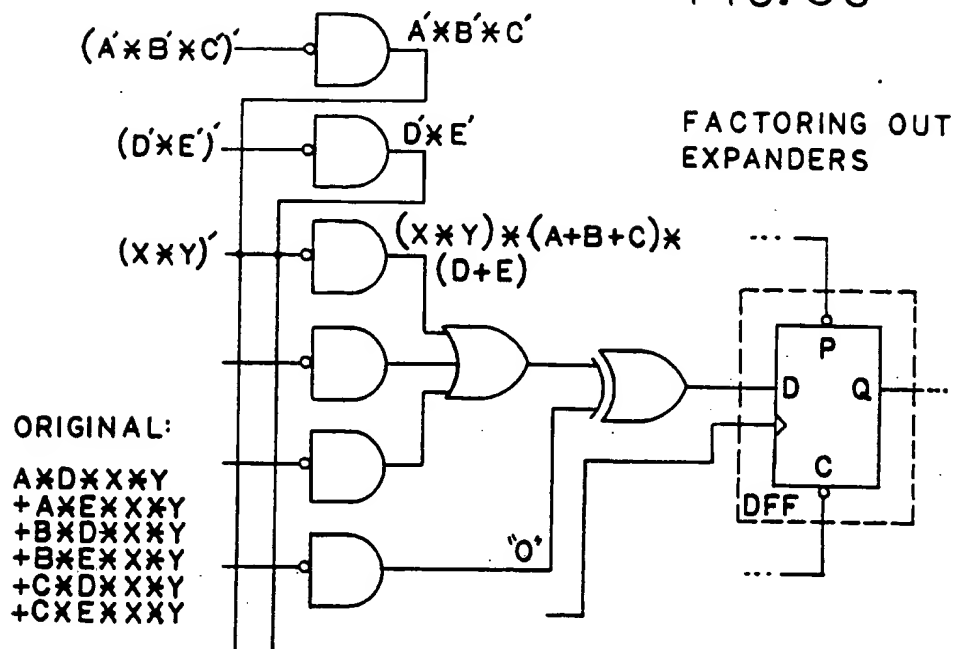
ORIGINAL: SYNTHESIZED AS:

FITTING DIRECTLY



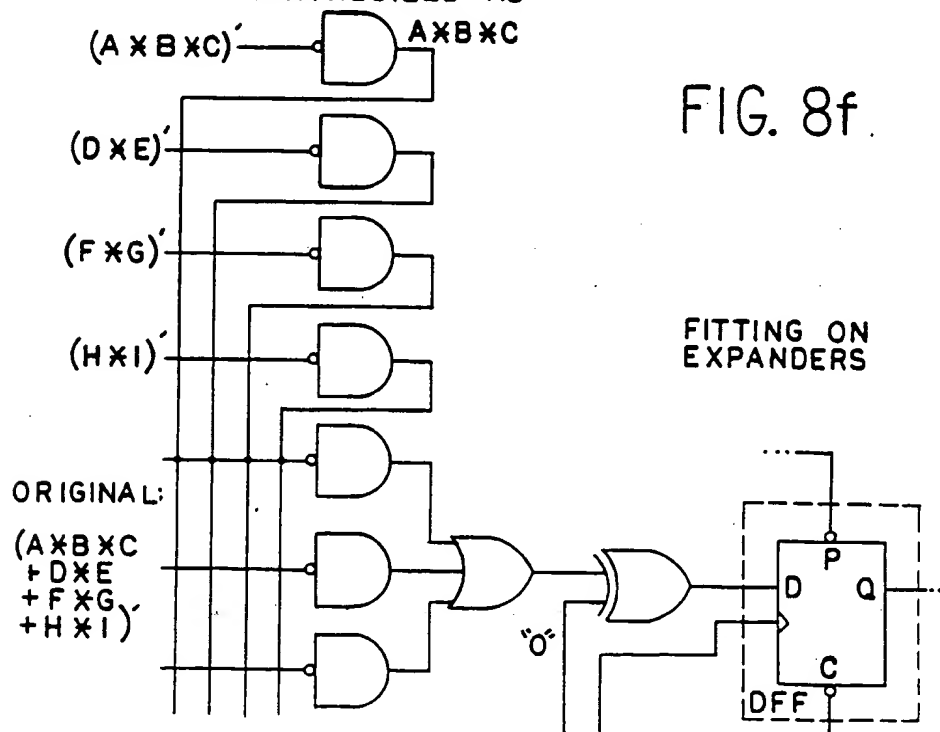
SYNTHESIZED AS:

FIG. 8e



SYNTHESIZED AS:

FIG. 8f.





SYNTHESIZED AS:

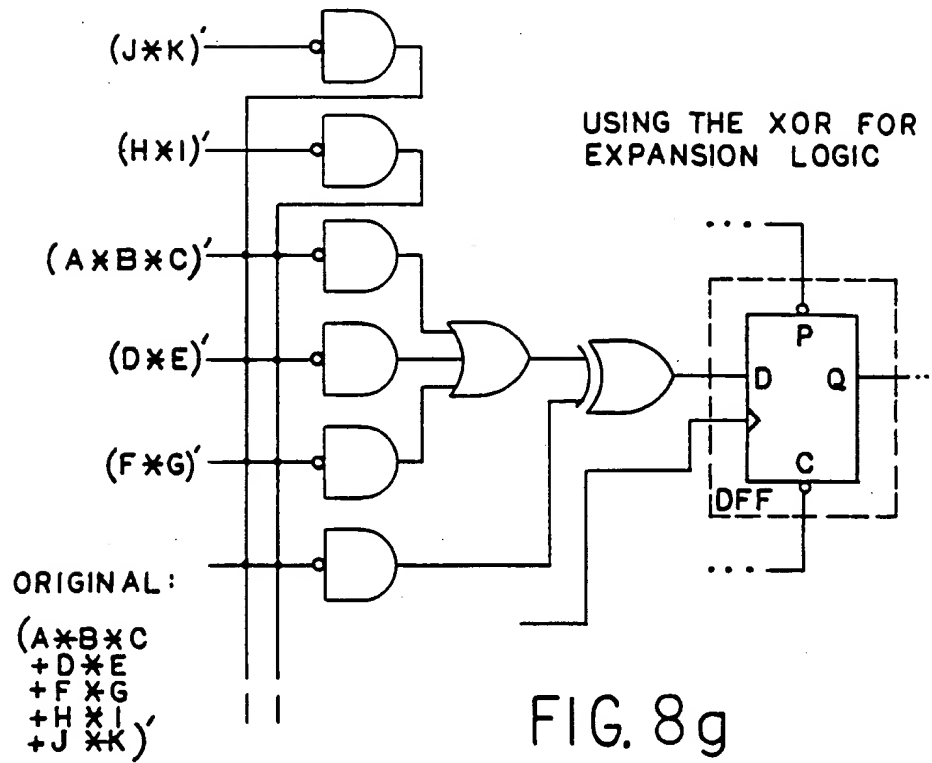


FIG. 8h

